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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/172,553	10/14/98	GREEN J	2914.IUS

EXAMINER	
DIAZ, J	
ART UNIT	**PAPER NUMBER**
2815	

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DATE MAILED: 07/17/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/172,553	GREEN ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-35 and 37-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-35, 37-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

➢ Claims 31-35, 37-38 and 40-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn et al. (US Patent No. 5,358,888).

Regarding claim 31, Ahn et al. teach a semiconductor capacitor storage poly (see columns 1-12) including downwardly extending recesses (See Figure 19), and a plurality of contiguous mesas (80) forming a maze-like structure (100) (See Figures 6, 16 and 19).

Regarding claim 32, Ahn et al. teach that said mesas extend in the X, Y and Z coordinates (See Figures 6, 16 and 19).

Regarding claim 33, Ahn et al. teach a semiconductor capacitor storage poly (see columns 1-12) including downwardly extending recesses (see openings formed in layer 40 of Figure 19); a plurality of contiguous webs (see pattern formed below HSG 80 of Figure 19) forming a maze-like structure (100) (See Figures 6, 16 and 19); and hemispherical-grain polysilicon (80) (see Figure 19).

Regarding claim 34, Ahn et al. teaches that said webs extend in the X, Y and Z coordinates (See Figures 6, 8 and 16).

Regarding claims 35 and 43, Ahn et al. teach an intermediate semiconductor capacitor structure (see columns 1-12), comprising: a storage poly structure (40) with recesses formed therein (see openings formed in layer 40 of Figure 18); and a hemispherical-grain polysilicon layer (80) over said storage poly structure (see Figure 18); a mask (70) (see Figure 18).

Regarding claim 37, Ahn et al. teach an intermediate semiconductor memory cell structure (see columns 1-12), comprising: a storage poly structure (40) (see Figure 18); low elevation regions of a hemispherical-grain polysilicon layer (80) on said storage poly structure (see Figure 18); recesses (see openings formed in layer 40 of Figure 18); and dielectric material (56) at least lining the recesses (see Figure 18).

Regarding claims 38 and 41, Ahn et al. teach an intermediate semiconductor memory cell structure (see columns 1-12), comprising: a storage poly structure (40) (see Figure 18); low elevation regions of a hemispherical-grain polysilicon layer (80) on said storage poly structure (see Figure 18); recesses (see openings formed in layer 40 of Figure 18); and dielectric material (56) substantially coating an upper surface of said storage poly structure and at least lining the recesses (see Figure 18).

Regarding claim 40, Ahn et al. teach said poly structure has web-like structure webs (see pattern formed below HSG 80 of Figure 19).

Regarding claim 42, Ahn et al. teach an intermediate semiconductor memory cell structure (see columns 1-12) comprising: a storage poly structure (40) (see Figure 18);

a substantially confluent hemispherical-grain polysilicon layer (80) (see Figure 18); and a mask (70) (see Figure 18).

Regarding claims 44-45, Ahn et al. teach an intermediate semiconductor memory cell structure (see columns 1-12) comprising: a storage poly structure (40) including recesses formed therein (see openings formed in layer 40 of Figure 18); low elevation regions of a hemispherical-grain polysilicon layer (80) (see Figure 18); a mask (70) (see Figure 18); and a dielectric material (56) (see Figure 18).

➢ Claims 38-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Batra et al. (US Patent No. 6,060,355).

Regarding claims 38 and 40-41, Batra et al. teach an intermediate semiconductor memory cell structure (see columns 1-8), comprising: a storage poly structure (50,86) (see Figure 6); low elevation regions of a hemispherical-grain polysilicon layer (86) on said storage poly structure (see Figure 6); recesses (see openings formed between hemispherical-grain polysilicon layer 86 in Figure 6); and dielectric material (90) substantially coating an upper surface of said storage poly structure and at least lining the recesses (see Figure 6).

Regarding claim 39, Park teaches a cell poly structure (92) (See Figure 6).

Response to Arguments

➢ Applicant's arguments with respect to claims 31-35, 37-45 have been considered but are moot in view of the new ground(s) of rejection.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
July 16, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800